Preliminary

Product Information

ISSUE DATA : 2008-09-09
MODEL : LMS350DF01

Note : The Product and specifications are subject to change without any notice. Please ask for the latest Product Standards to guarantee the satisfaction of your product requirements.

PREPARED BY : AM LCD Mobile Display Development

Samsung Electronics Co. , LTD.

심주환020205881225177167 20080909144125
306931220938848

Contents

Revision History ---------- (3)
General Description ---------- (4)
1. Absolute Maximum Ratings ---------- (5)
1.1 Absolute Ratings Of Environment
1.2 Electrical Absolute Ratings
2. Optical Characteristics ---------- (7)
3. Electrical Characteristics ---------- (10)
3.1 TFT-LCD Module
3.2 Back-light Unit
4. Block Diagram ---------- (11)
4.1 TFT-LCD Module with Back Light Unit
4.2 Back Light Unit
5. Input Terminal Pin Assignment ---------- (12)
5.1 Input Signal & Power
5.2 Input Signal, Basic Display Colors and Gray Scale of Each Colors
6. Operation Specifications ---------- (14)
6.1 Dot Formation
6.2 Data Format for 24 bit RGB interface
7. Interface Timing ---------- (15)
7.1 24bit RGB Interface Timing
7.2 Serial Peripheral Interface
8. Electrical Specifications ---------- (17)
9. Power Sequence ---------- (19)
9.1 Power on Sequence
9.2 Power off Sequence
9.3 Standby In / Out Sequence
10. Application Circuit ---------- (23)
11. Module Outline Dimension ---------- (24)
12. Packing ---------- (25)
13. Marking and Others ---------- (26)
14. General Precaution ---------- (27)
14.1 Handling
14.2 Storage
14.3 Operation
14.4 Others

심주환020205881225177167 20080909144125

306931220938848

Revision History

Data	Rev. No.	Page	Summary
July. 07. 2008	000		Rev.000 was first issued.
		20	Power sequence updated. (RED text)
		24	FPC silk removed. (only top)
Aug. 28. 2008		24	Cover Pad added.
.			

심주환020205881225177167 20080909144125
306931220938848

General Description

* Description

LMS350DF01-001 is a TMR(Transmissive with Micro Reflective) type color active matrix TFT (Thin Film Transistor) liquid crystal display (LCD) that uses amorphous silicon TFT as a switching devices. This model is composed of a TFT-LCD module, a driver circuit and a back-light unit. The resolution of a 3.5" contains 320 x 480 dots and can display up to 16,777,216 colors.

* Features

- Transmissive with Micro Reflective type and back-light with 5LEDs.
- mPVA mode (Normally Black).
- Wide Viewing Angle.
- Stripe Pixel structure.
- 24bit RGB Interface + Serial Peripheral Interface (SPI)
- Gate Driver IC embeded on Panel
- Low Power consumption.

* Applications

- Display terminals for MP3, PMP application products.

*** General information**

Items	Specification	Unit	Note
Display Area	48.96(H) x 73.44(V)	mm	-
Driver Element	a-Si TFT active matrix	-	-
Display Colors	16.7 M	color	-
Number of Pixels	320(H) x 480(V)	pixel	-
Pixel Arrangement	Stripe Structure	-	-
Pixel Pitch	0.153(H) x 0.153(V)	mm	-
Display Mode	Normally Black	-	-

*** Mechanical information**

Item		Min.	Typ.	Max.	Unit	Note
Module size	Horizontal(H)	54.56	54.76	54.96	mm	(1)
	Vertical(V)	83.04	83.24	83.44	mm	(1)
	Depth(D)	1.63	1.83	2.03	mm	(1)
Weight		-	13	-	g	(2)

Note (1) : Not include FPC

Note (2) : Included FPC

심주환020205881225177167 20080909144125

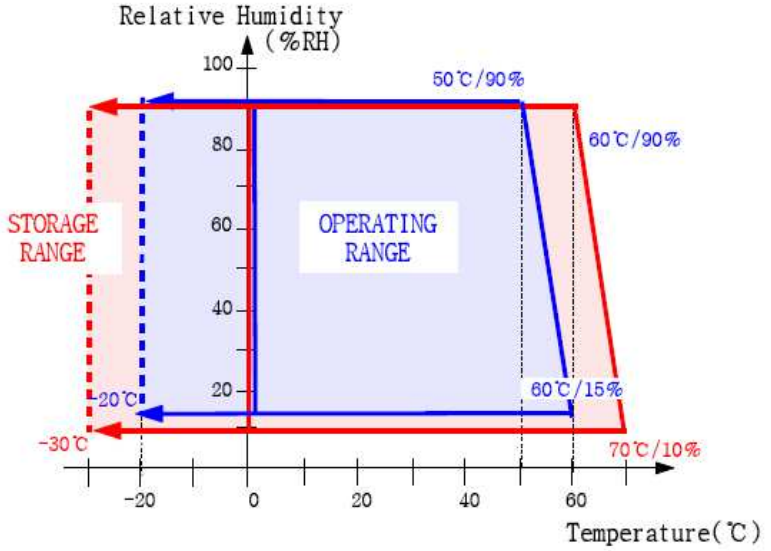
306931220938848

1. Absolute Maximum Ratings

1.1 Absolute Ratings of Environment

Item	Symbol	Min.	Max.	Unit	Note
Storage temperature	TSTG	-30	70	℃	(1)
Operating temperature (Ambient temperature)	TOPR	-20	60	℃	(1),(2)

Note (1) 90 % RH Max. (50℃ ³ Ta)
Maximum wet-bulb temperature at 49℃ or less. (Ta > 50℃)
No condensation.



Temperature & Humidity Graph at Absolute Environment

(2) In case of below 0℃, the response time of liquid crystal (LC) becomes slower and the color of panel becomes darker than normal one. Level of retardation depends on temperature, because of LC's characteristics.

(3) If any fixed pattern is displayed on LCD for minutes, image-sticking phenomenon may occur.

심주환020205881225177167 20080909144125
306931220938848

1.2 Electrical Absolute Ratings

(1) TFT-LCD Module

(Ta = 25℃ ± 2℃, GND=0V)

Characteristics	Symbol	Min.	Max.	Unit	Note
Logic Input Voltage	VDD3	-0.3	5.0	V	(1)
Analog Input Voltage	VCI	-0.3	5.0	V	(1)

(2) Back-Light Unit

(Ta = 25 ± 2℃)

Item	Symbol	Min.	Max.	Unit.	Note
Current	I_B	-	25	mA	(1)

Note (1) Permanent damage to the device may occur if maximum values are exceeded or reverse voltage is loaded.
Functional operation should be restricted to the conditions described under normal operating conditions.

심주환020205881225177167 20080909144125
306931220938848

2. Optical Characteristics

The following items are measured under stable conditions. The optical characteristics should be measured in a dark room or equivalent state with the methods shown in Note (1). Measuring equipment: SR-3, BM-7, EZ-Contrast

(Ta = 25 ± 2°C, VDD3 = VCI = 3.3V, I_B = 20mA)

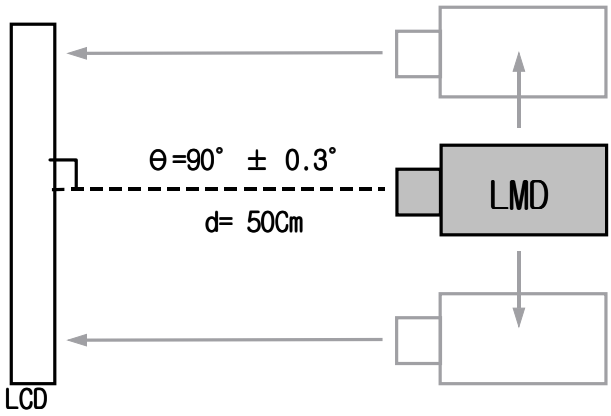
Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Contrast ratio (Center point)		C/R	Note (1),(6) Φ = 0 Θ = 0 Normal Viewing Angle B/L On	500	800	-	-	(2) SR-3
Luminance of white (Center point)		Y_L		285	380	-	cd/m²	(3) SR-3
Response time	Rising: Tr	Tr+Tf		-	30	35	msec	(4) BM-7
	Falling: Tf							
Color chromaticity (CIE 1931)	White	Wx		0.270	0.320	0.370	-	(5) SR-3
		Wy		0.297	0.347	0.397		
	Red	Rx		0.555	0.605	0.655		
		Ry		0.278	0.328	0.378		
	Green	Gx		0.278	0.328	0.378		
		Gy		0.533	0.583	0.633		
	Blue	Bx		0.101	0.151	0.201		
		By		0.061	0.111	0.161		
Viewing angle	Hor.	ΘL	C/R≥10 B/L On	80	-	-	Degrees	(6) Ez - Contrast
		ΘR		80	-	-		
	Ver.	ΦH		80	-	-		
		ΦL		80	-	-		

심주환020205881225177167 20080909144125
306931220938848

Note (1) Test Equipment Setup

After stabilizing and leaving the panel alone at a given temperature for 30 min, the measurement should be executed. Measurement should be executed in a stable, windless, and dark room. 30 min after lighting the back-light. This should be measured in the center of screen.

- **Environment condition : Ta = 25 ± 2 ℃**
- **Back-Light On condition**



LMD : Ligh Mesurement Devices

Note (2) Definition of Contrast Ratio (C/R) : Ratio of gray max (Gmax) & gray min (Gmin) at the center point

$$CR = \frac{G\ max}{G\ min}$$

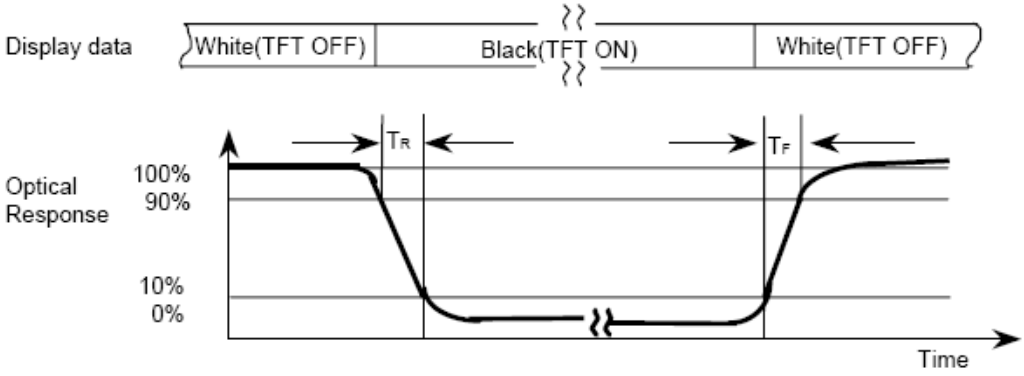
*** Gmax : Luminance with all dots white**
*** Gmin : Luminance with all dots black**

심주환020205881225177167 20080909144125
306931220938848

Note (3) Definition of Luminance of White (YL)

: Luminance of white at the center point

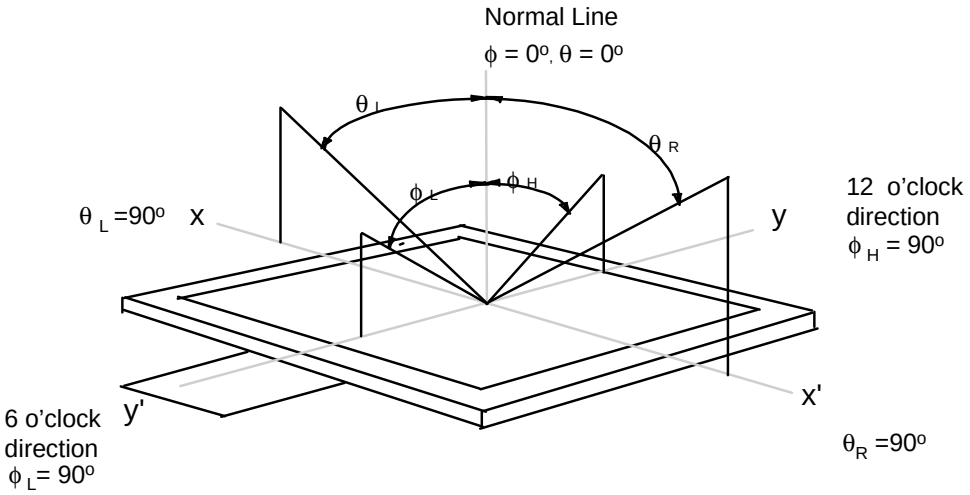
Note (4) Definition of Response time : Sum of Tr and Tf (Field : 1)



Note (5) Definition of Color Chromaticity (CIE 1931)

Color coordinate of white & red, green, blue at center point.

Note (6) Definition of Viewing Angle : Viewing angle range (CR≥10)



심주환020205881225177167 20080909144125
306931220938848

3. Electrical Characteristics

3.1 TFT-LCD Module

Ta = 25 ± 2℃

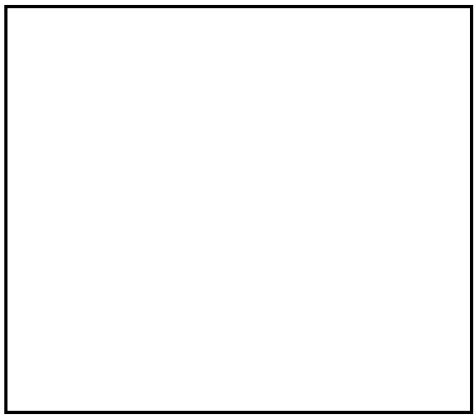
Characteristics	Symbol	Min.	Typ.	Max.	Unit	Note
Logic Input Voltage	VDD3	3.25	3.3	3.35	V	-
Analog Input Voltage	VCI	3.25	3.3	3.35	V	-
Power Dissipation	I_{FULL}	-	25	30	mA	(1),(2)
	Istandby		30	100	uA	
Frame frequency	f_{Frame}	-	60	-	Hz	-
Dot Clock	DCK	-	10	-	MHz	-
Serial Clock	XSCK	-	-	10	MHz	-

*** To prevent a latch-up or DC operation of the LCD module, the power on/off sequence should be as the Chapter 10. Power On/Off Sequence.**

Note (1) VDD3 = VCI = 3.3V f_{Frame} = 60 Hz

(2) Dissipation current check pattern

▶ White pattern



심주환020205881225177167 20080909144125
306931220938848

3.2 Back-Light unit

The back-light system is an edge-lighting type with five white LED (Light Emitting Diode)s.

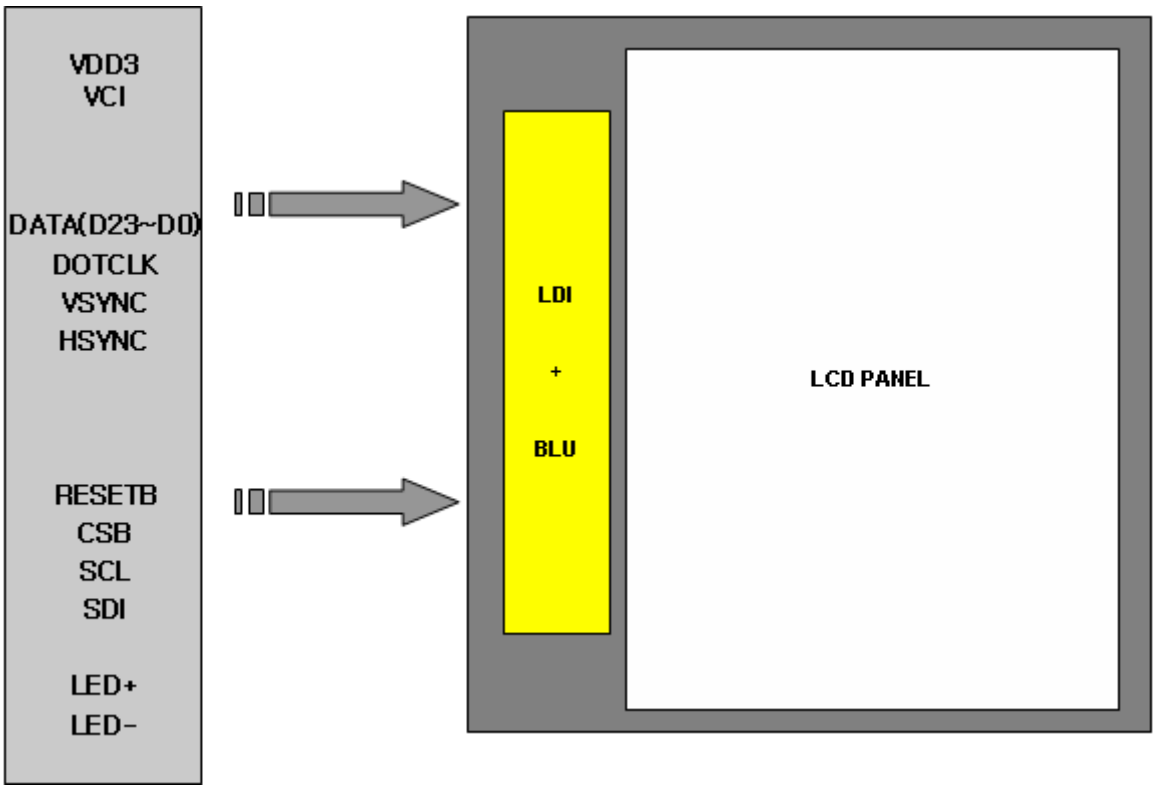
(Ta=25 ± 2°C)

Item	Symbol	Min.	Typ.	Max.	Unit	Note
Current	I_B	-	20	-	mA	(1)
Power Consumption	P_{BL}	-	330	-	mW	-

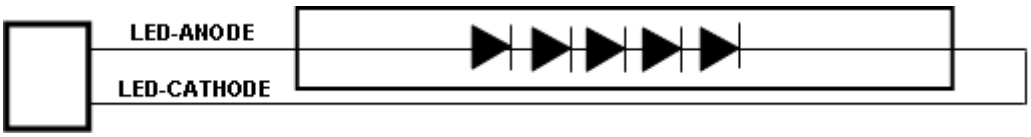
Note (1) Five LEDs serial type.

4. Block Diagram

4.1 TFT-LCD Module (Interface System Structure)



4.2 Back Light Unit



심주환020205881225177167 20080909144125
306931220938848

5. Input Terminal Pin Assignment

5.1 Input Signal & Power (BTB Connector: DF30FC-70DS-0.4V)

Pin No	Symbol	Description	I/O	Pin No	Symbol	Description	I/O
1	LED+	LED Anode	I	36	VCI	Analog Input Voltage	I
2	GND	Ground	I	37	PD10	GREEN 2	I
3	NC	No Connectior	-	38	VCI	Analog Input Voltage	I
4	VGOFFL	Power Output for ASG driver	O	39	PD9	GREEN 1	I
5	LED-	LED Cathode	I	40	C23M	Charge Pumping Capacitor	O
6	GND	Ground	I	41	PD8	GREEN 0	I
7	GND	Ground	I	42	C23P	Charge Pumping Capacitor	O
8	VGL	Gate Off Voltage	O	43	GND	Ground	I
9	PD23	RED 7	I	44	VCL	Power Supply for Generating VCOML	O
10	GND	Ground	I	45	PD7	BLUE 7	I
11	PD22	RED 6	I	46	VSSA	Ground	I
12	VGH	Gate On Voltage	O	47	PD6	BLUE 6	I
13	PD21	RED 5	I	48	VCOMH	VCOM High Level	O
14	C22P	Charge Pumping Capacitor	O	49	PD5	BLUE 5	I
15	PD20	RED 4	I	50	VCOML	VCOM Low Level	O
16	C22M	Charge Pumping Capacitor	O	51	PD4	BLUE 4	I
17	PD19	RED 3	I	52	GVDD	Gamma Voltage Generator	O
18	C21P	Charge Pumping Capacitor	O	53	PD3	BLUE 3	I
19	PD18	RED 2	I	54	RVDD	Regulated VDD output	O
20	C21M	Charge Pumping Capacitor	O	55	PD2	BLUE 2	I
21	PD17	RED 1	I	56	VDD3	Logic Input Voltage	I
22	AVDD	Power Output for Source Driver	O	57	PD1	BLUE 1	I
23	PD16	RED 0	I	58	VDD3	Logic Input Voltage	I
24	C11Pb	Charge Pumping Capacitor	O	59	PD0	BLUE 0	I
25	GND	Ground	I	60	VSYNC	Vsync	I
26	C11Mb	Charge Pumping Capacitor	O	61	GND	Ground	I
27	PD15	GREEN 7	I	62	HSYNC	Hsync	I
28	C11P	Charge Pumping Capacitor	O	63	DOTCLK	Dotclk	I
29	PD14	GREEN 6	I	64	SCL	Serial Clock	I
30	C11M	Charge Pumping Capacitor	O	65	SDI	Serial Data Input	I
31	PD13	GREEN 5	I	66	CSB	Chip Select	I
32	VSSC	Ground	I	67	ENABLE	Ground	I
33	PD12	GREEN 4	I	68	RESETB	Reset	I
34	VCI1	Reference Voltage In Step Up Circuit	O	69	GND	Ground	I
35	PD11	GREEN 3	I	70	GND	Ground	I

심주환020205881225177167 20080909144125
306931220938848

5.2 Input Signal, Basic Display Colors and Gray Scale of Each Colors

COLOR	DISPLAY	DATA SIGNAL																								GRAY SCALE LEVEL
		RED								GREEN								BLUE								
		R0	R1	R2	R3	R4	R5	R6	R7	G0	G1	G2	G3	G4	G5	G6	G7	B0	B1	B2	B3	B4	B5	B6	B7	
BASIC COLOR	BLACK	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	-
	BLUE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	-
	GREEN	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	-
	CYAN	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	-
	RED	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	-
	MAGENTA	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	-
	YELLOW	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	-
	WHITE	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	-
GRAY SCALE OF RED	BLACK	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	R0
	DARK ↑	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	R1
		0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	R2
		:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	R3~R252
	↓ LIGHT	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	
		1	0	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	R253
		0	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	R254
	RED	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	R255
GRAY SCALE OF GREEN	BLACK	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	G0
	DARK ↑	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	G1
		0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	G2
		:			:	:	:	:	:	:			:	:	:	:	:	:			:	:	:	:	:	G3~G252
	↓ LIGHT	:			:	:	:	:	:	:			:	:	:	:	:	:			:	:	:	:	:	
		0	0	0	0	0	0	0	0	1	0	1	1	1	1	1	1	0	0	0	0	0	0	0	0	G253
		0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	G254
	GREEN	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	G255
GRAY SCALE OF BLUE	BLACK	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	B0
	DARK ↑	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	B1
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	B2
		:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	B3~B252
	↓ LIGHT	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	1	1	1	1	1	B253
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	B254
	BLUE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	B255

Note) Definition of Gray :

Rn : Red Gray, Gn : Green Gray, Bn : Blue Gray (n = Gray level)

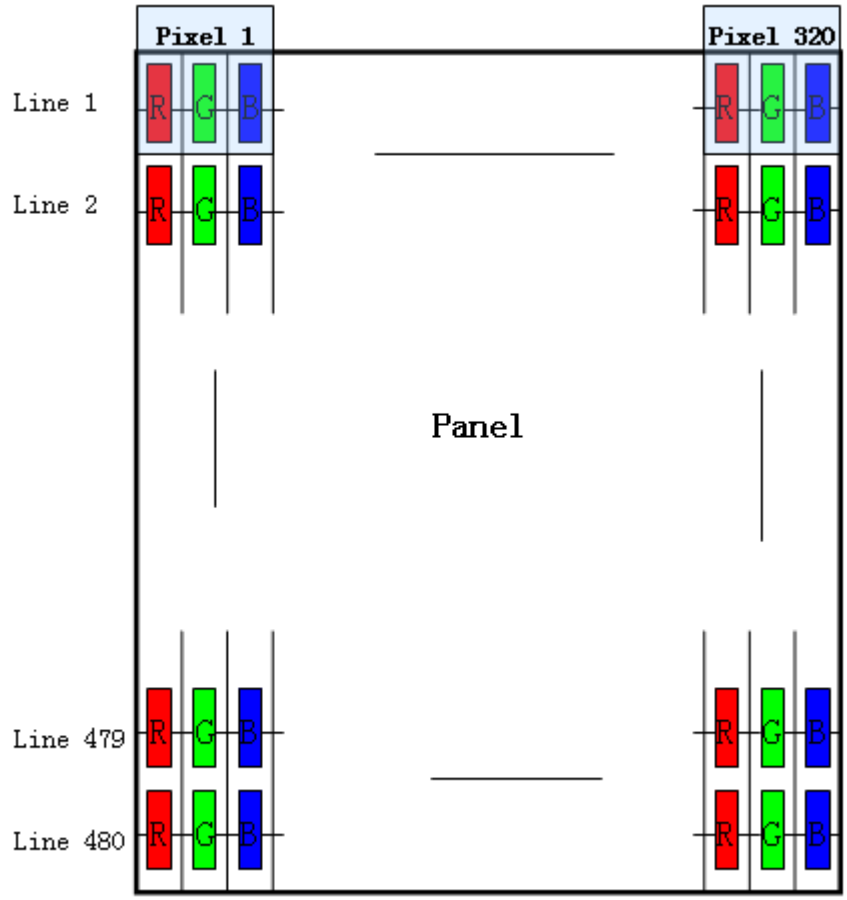
Input Signal : 0 = Low level voltage, 1 = High level voltage

심주환020205881225177167 20080909144125

306931220938848

6. Operation Specifications

6.1 Pixel Formation (Stripe Pixel Structure)



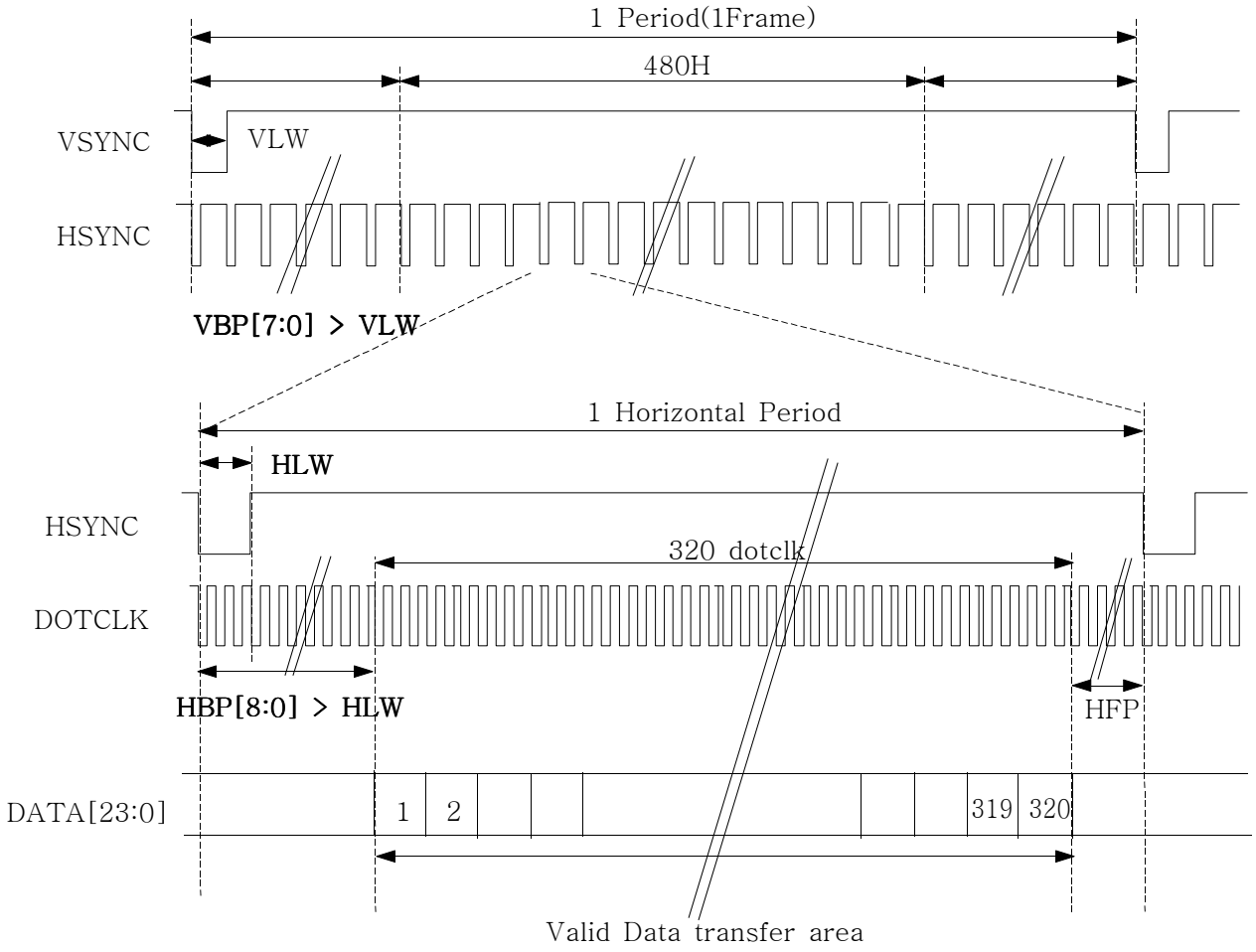
6.2 Data Format for 24bit RGB Interface

Input	D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
RGB Assingment	R7	R6	R5	R4	R3	R2	R1	R0	G7	G6	G5	G4	G3	G2	G1	G0	B7	B6	B5	B4	B3	B2	B1	B0

심주환020205881225177167 20080909144125
306931220938848

7. Interface Timing

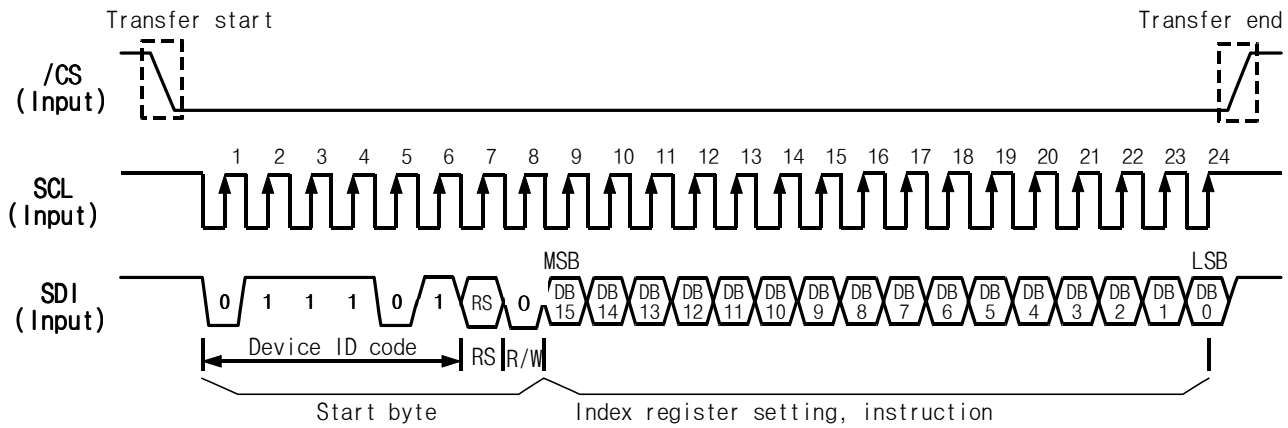
7.1 24bit RGB Interface Timing



* DOTCLK = f_{frame} × (480 + VBP + VFP) × (320 + HBP + HFP)
  = (60)Hz × (480 + VBP + VFP) × (320 + HBP + HFP)
* VBP ≥ 3 , VBP > VLW ≥ 2
* HBP ≥ 8 , HBP > HLW ≥ 2

심주환020205881225177167 20080909144125
306931220938848

7.2 Serial Peripheral Interface



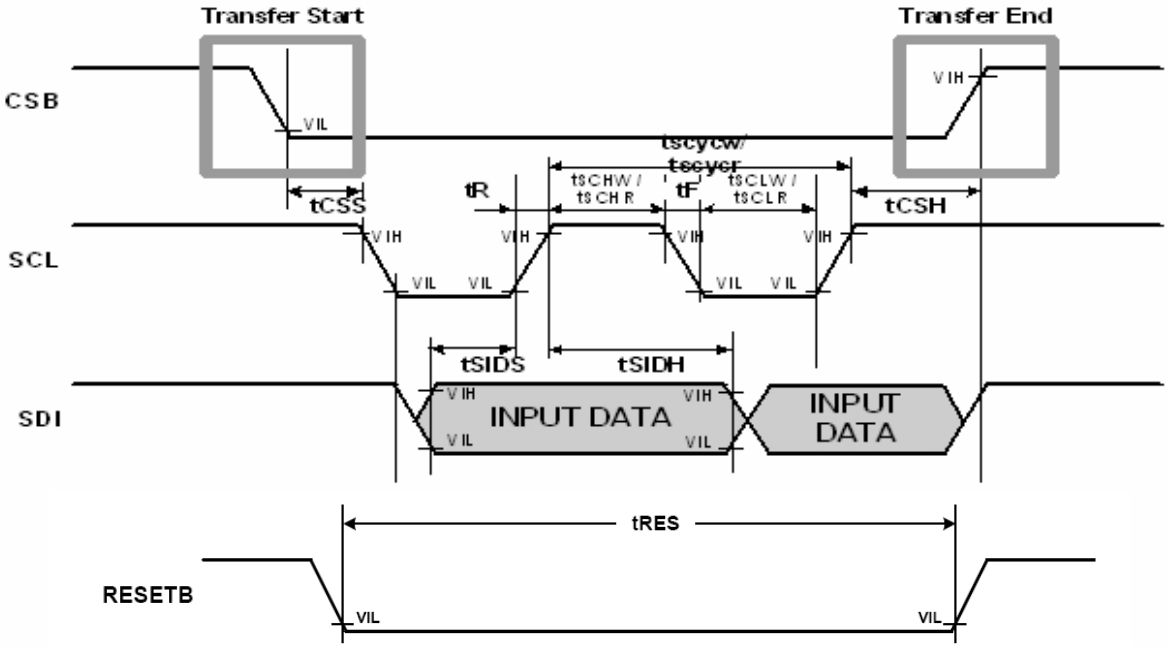
(Note) RS="0": Index data
RS="1": Instruction data

심주환020205881225177167 20080909144125
306931220938848

8. Electrical Specifications

VDD3 = 3.3V, Ta = 25℃ ± 2℃

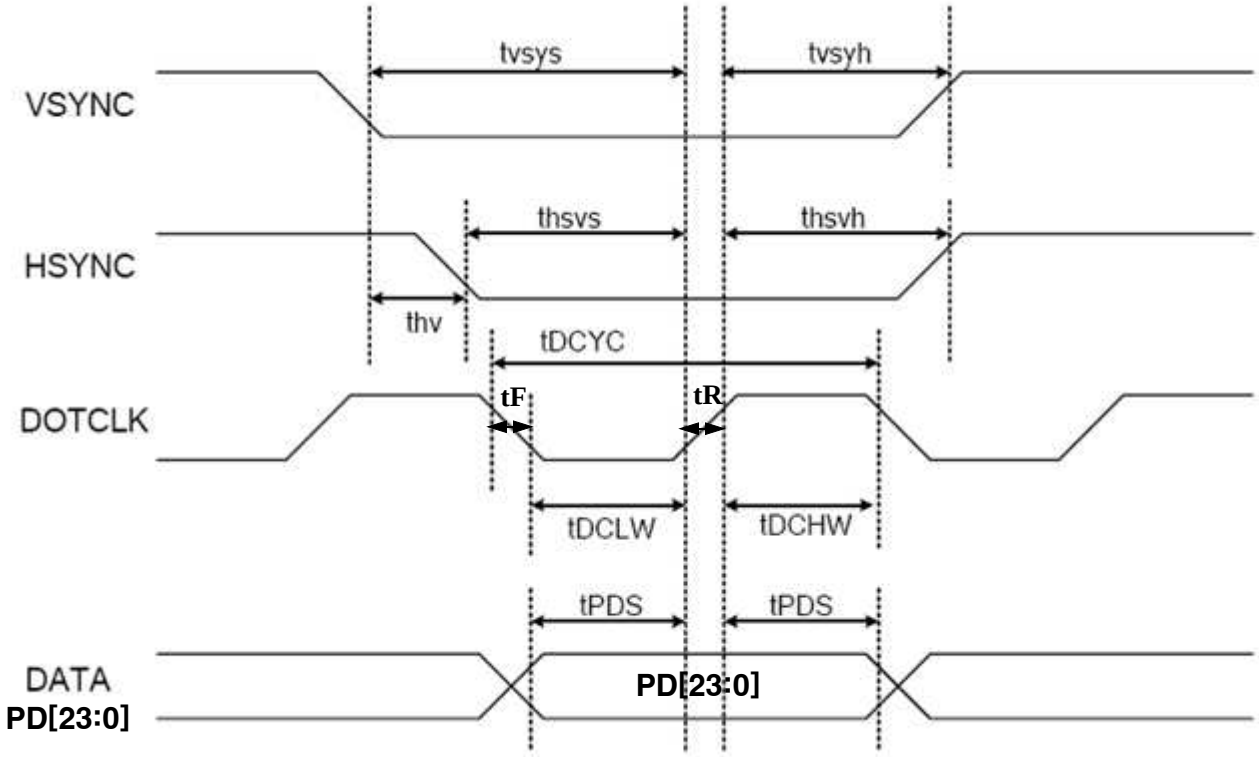
Item	Symbol	Min.	Max.	Unit
Serial Clock Cycle Time(write)	tSCYCW	100	-	ns
Serial Clock rise/fall time	tR,tF	-	10	
Pulse width high for write	tSCHW	30	-	
Pulse width low for write	tSCLW	50		
Chip Select Setup Time	tCSS	20	-	
Chip Select Hold Time	tCSH	90	-	
Serial Input Data Setup Time	tSIDS	30	-	
Serial Input Data Hold Time	tSIDH	30	-	
Serial Output Data delay Time	tSODD	-	200	
Serial Output Data Hold Time	tSODH	5	-	
Reset Low Pulse Width	tRES	30	-	us
CSB Low Pulse Width for Wake up	tCSBR	12	-	



심주환020205881225177167 20080909144125
306931220938848

VDD3 = 3.3V, Ta = 25℃ ± 2℃

Item	Symbol	Min.	Max.	Unit
Vsync/Hsync Setup Time	Tvsys Thsvs	20	-	ns
Vsync/Hsync Hold Time	Tvsyh Thsyh	20	-	
Dotclk Low Level Pulse Width	tDCLW	50	-	
Dotclk High Level Pulse Width	tDCHW	50	-	
Dotclk Cycle Time	tDCYC	100	-	
PD(Data) Setup Time	tPDS	12	-	
PD(Data) Hold Time	tPDH	12	-	
Dotclk Rise/Fall Time	tR, tF	-	10	



심주환020205881225177167 20080909144125
306931220938848

. Power On/Off Sequence (*Can be changed for better quality)

9.1 Power On Sequence

POWER ON Sequence

Wait 1ms

/ RESET
R07h = 0000

Wait more than 10ms

R11h = 222F
R12h = 0F00
R13h = 7FE3
R76h = 2213
R74h = 0001
R76h = 0000
R10h = 560C

Wait more than 6frames

R12h = 0C63

Wait more than 5frames

R01h = 0B3B (note1)
R02h = 0300
R03h = C040(note2)
R08h = 0004(note3)
R09h = 000B(note4)
R76h = 2213
R0Bh = 3340
R0Ch = 0020
R1Ch = 7770
R76h = 0000
R0Dh = 0000
R0Eh = 0500
R14h = 0000
R15h = 0803
R16h = 0000
R30h = 0005
R31h = 070F
R32h = 0300
R33h = 0003
R34h = 090C
R35h = 0001
R36h = 0001
R37h = 0303
R38h = 0F09
R39h = 0105

DISPLAY ON Sequence

R07h = 0001

Wait more than 1frame

R07h = 0101

Wait more than 2frame

R07h = 0103

Display ON

심주환020205881225177167 20080909144125
306931220938848

9.2 Power Off Sequence

R10h = 0001
R0Bh = 30E1
R07h = 0102

Wait more than 2frames

R07h = 0000
R12h = 0000
R10h = 0100

Power OFF

9.3 Standby In / Out Sequence

Display On Status

Display Off Sequence

R10h = 0001

Standby IN

Standby In Status

R10h = 0000

Power On Sequence

Display On Sequence

Standby OUT

심주환020205881225177167 20080909144125
306931220938848

Note 1) Inversion Setting

DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	BGR	0	TB	SS	0	0	1	1	1	0	1	1

*** BGR : Color Inversion (0 : R ↔ B, 1 : bypass)**

*** TB : Vertical Inversion (0 : Bottom → Top, 1 : Top → Bottom)**

*** SS : Horizontal Inversion (0 : Right → Left, 1 : Left → Right)**

Note 2) Polarity Setting

DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
VPL	HPL	DPL	0	0	0	0	0	0	1	0	0	0	0	0	0

*** VPL : Vsync Polarity (0 : High Active, 1 : Low Active)**

*** HPL : Hsync Polarity (0 : High Active, 1 : Low Active)**

*** DPL : Dotclk Polarity (0 : Data fetched at falling edge, 1 : at rising edge)**

Note 3) VBP (Vsync Back Porch)

DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	0	VBP7	VBP6	VBP5	VBP4	VBP3	VBP2	VBP1	VBP0

VBP 7	VBP 6	VBP 5	VBP 4	VBP 3	VBP 2	VBP 1	VBP 0	Number of Raster Periods In the Back Porch
0	0	0	0	0	0	0	0	3
0	0	0	0	0	0	0	1	3
0	0	0	0	0	0	1	0	4
0	0	0	0	0	0	1	1	5
0	0	0	0	0	1	0	0	6
			. . .					. . .
1	1	1	1	1	1	0	0	254
1	1	1	1	1	1	0	1	255
1	1	1	1	1	1	1	0	256
1	1	1	1	1	1	1	1	257

* The porch period should meet the following condition.

257H ≥ VBP ≥ 3H , VBP > VLW

심주환020205881225177167 20080909144125

306931220938848

Note 4) HBP (Hsync Back Porch)

DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	HBP8	HBP7	HBP6	HBP5	HBP4	HBP3	HBP2	HBP1	HBP0

HBP 8	HBP 7	HBP 6	HBP 5	HBP 4	HBP 3	HBP 2	HBP 1	HBP 0	Number of MCLKs In the Back Porch 24 bit (8 bit)
0	0	0	0	0	0	0	0	0	8 (24)
0	0	0	0	0	0	0	0	1	8 (24)
0	0	0	0	0	0	0	1	0	8 (24)
0	0	0	0	0	0	0	1	1	8 (24)
0	0	0	0	0	0	1	0	0	8 (24)
0	0	0	0	0	0	1	0	1	8 (24)
0	0	0	0	0	0	1	1	0	8 (24)
0	0	0	0	0	0	1	1	1	8 (24)
0	0	0	0	0	1	0	0	0	8 (24)
0	0	0	0	0	1	0	0	1	9 (27)
0	0	0	0	0	1	0	1	0	10 (30)
0	0	0	0	0	1	0	1	1	11 (33)
				. . .					
1	1	1	1	1	1	1	0	1	509 (1527)
1	1	1	1	1	1	1	1	0	510 (1530)
1	1	1	1	1	1	1	1	1	511 (1533)

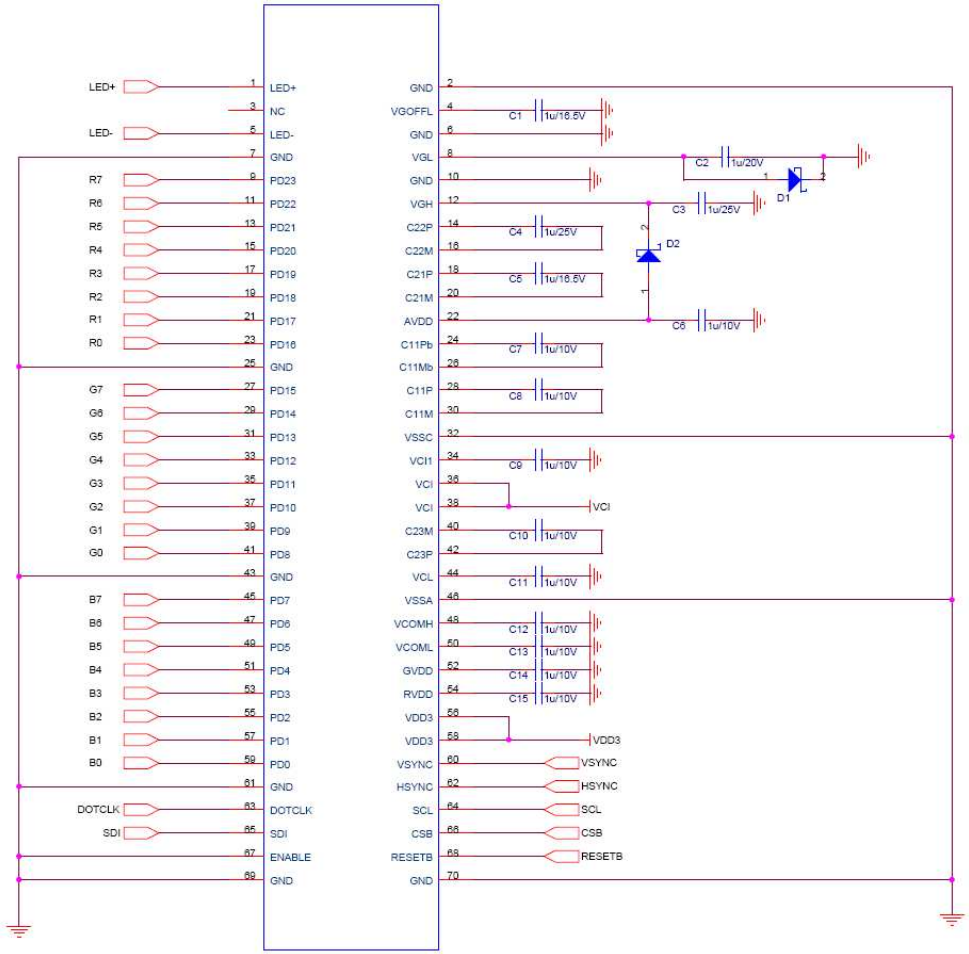
* The porch period should meet the following condition.
511dck ≥ HBP ≥ 8dck , HBP > HLW

Note 5) RIM

DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0					RIM4	RIM3	RIM2	RIM1	RIM0

심주환020205881225177167 20080909144125
306931220938848

10. Application Circuit



※ Recommands

1. All components would better be close to FPC connector as possible.

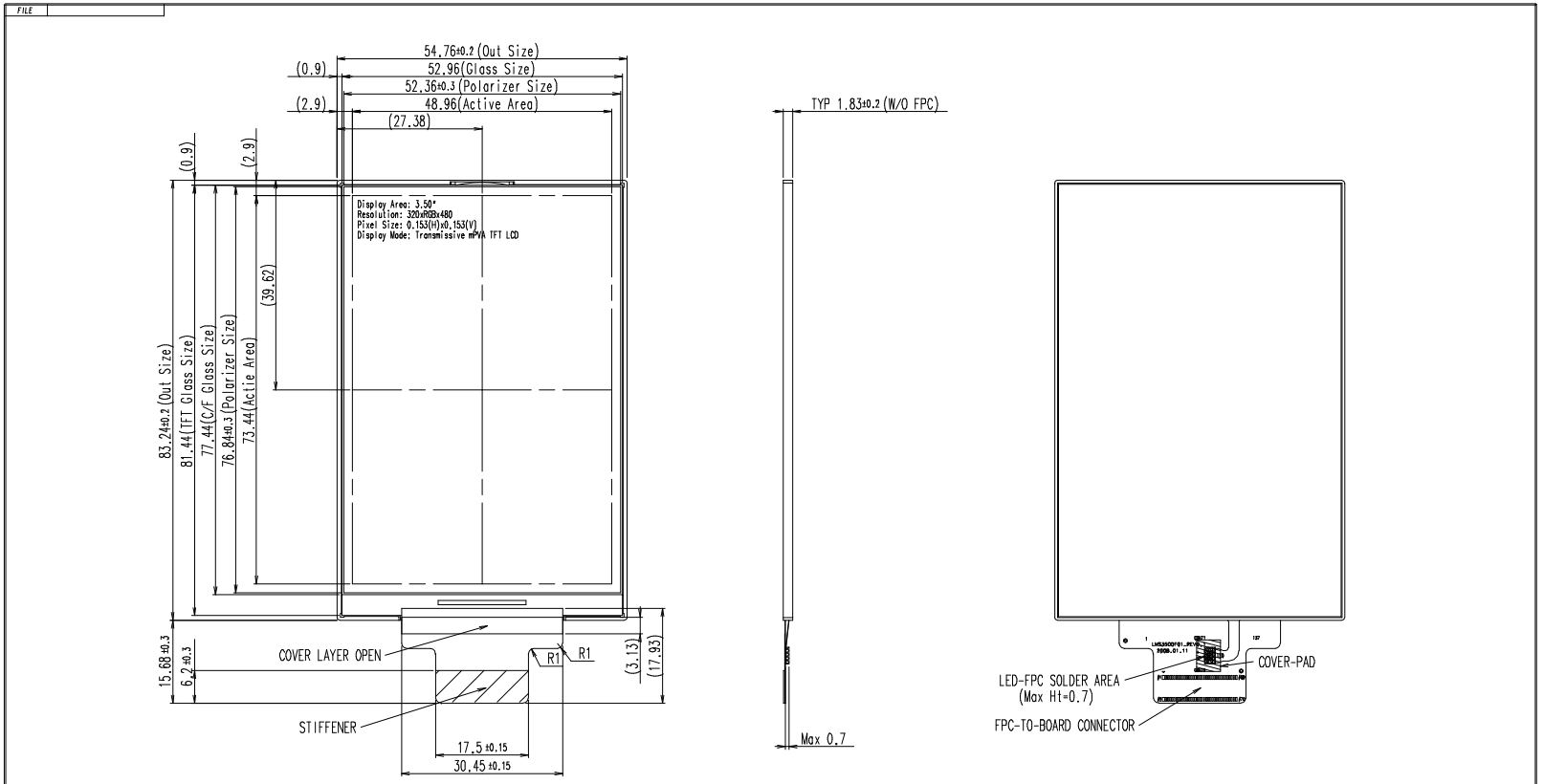
2. Schottky diode's low F/V(forward voltage) makes internal circuit more stable.

Name		Device	Value	Maximum Ratings Voltage
C1	VGOFFL	Capacitor	1uF	16.5V
C2	VGL	Capacitor	1uF	20V
C3	VGH	Capacitor	1uF	25V
C4	C22	Capacitor	1uF	25V
C5	C21	Capacitor	1uF	16.5V
C6	AVDD	Capacitor	1uF	10V
C7	C11b	Capacitor	1uF	10V
C8	C11	Capacitor	1uF	10V
C9	VCI1	Capacitor	1uF	10V
C10	C23	Capacitor	1uF	10V
C11	VCL	Capacitor	1uF	10V
C12	VCOMH	Capacitor	1uF	10V
C13	VCOML	Capacitor	1uF	10V
C14	GVDD	Capacitor	1uF	10V
C15	RVDD	Capacitor	1uF	10V
D1	VGL	Diode		Vf ≤ 0.28V (@IF =20mA, Ta = 25℃) VR ≥ max.25V)
D2	VGH	Diode		

심주환020205881225177167 20080909144125
306931220938848

Approval

11. Module outline Dimension



NOTE

1. DESCRIPTION : 3.5"(320X480) TM TFT DISPLAY
2. UNIT : mm
3. EJECTOR PIN AND GATE REMNANTS TO BE SUB-FLUSH
4. LCD MODULE BENDING ALLOWANCE SPEC : ±0.3
5. UNLESS OTHERWISE SPECIFIED TOLERANCE OF RADIUS : ±0.3
6. THIS MODULE IS ACCORDING TO ENVIRONMENTAL REQUIREMENTS(ROHS).

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF SAMSUNG ELECTRONICS. THE POSSESSOR AGREES TO THE FOLLOWING:
1) NOT TO REPRODUCE OR COPY
2) NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
3) ALL RIGHTS RESERVED

GENERAL TOLERANCE			
STEP	LEVEL 1	LEVEL 2	LEVEL 3
0 < X ≤ 4	±0.05	±0.1	±0.2
4 < X ≤ 16	±0.08	±0.15	±0.3
16 < X ≤ 64	±0.12	±0.25	±0.5
64 < X ≤ 256	±0.25	±0.4	±0.8

REV	DATE	DISCRIPTION OF REVISION	REASON	CHK'D BY

UNIT	mm	DRA'N BY	DES'D BY	CHK'D BY	APP'D BY
SCALE	1/1	S.I.CHANG			
TOLERANCE		'08.08.18			
LEVEL	3				

SAMSUNG ELECTRONICS

SPEC. NO

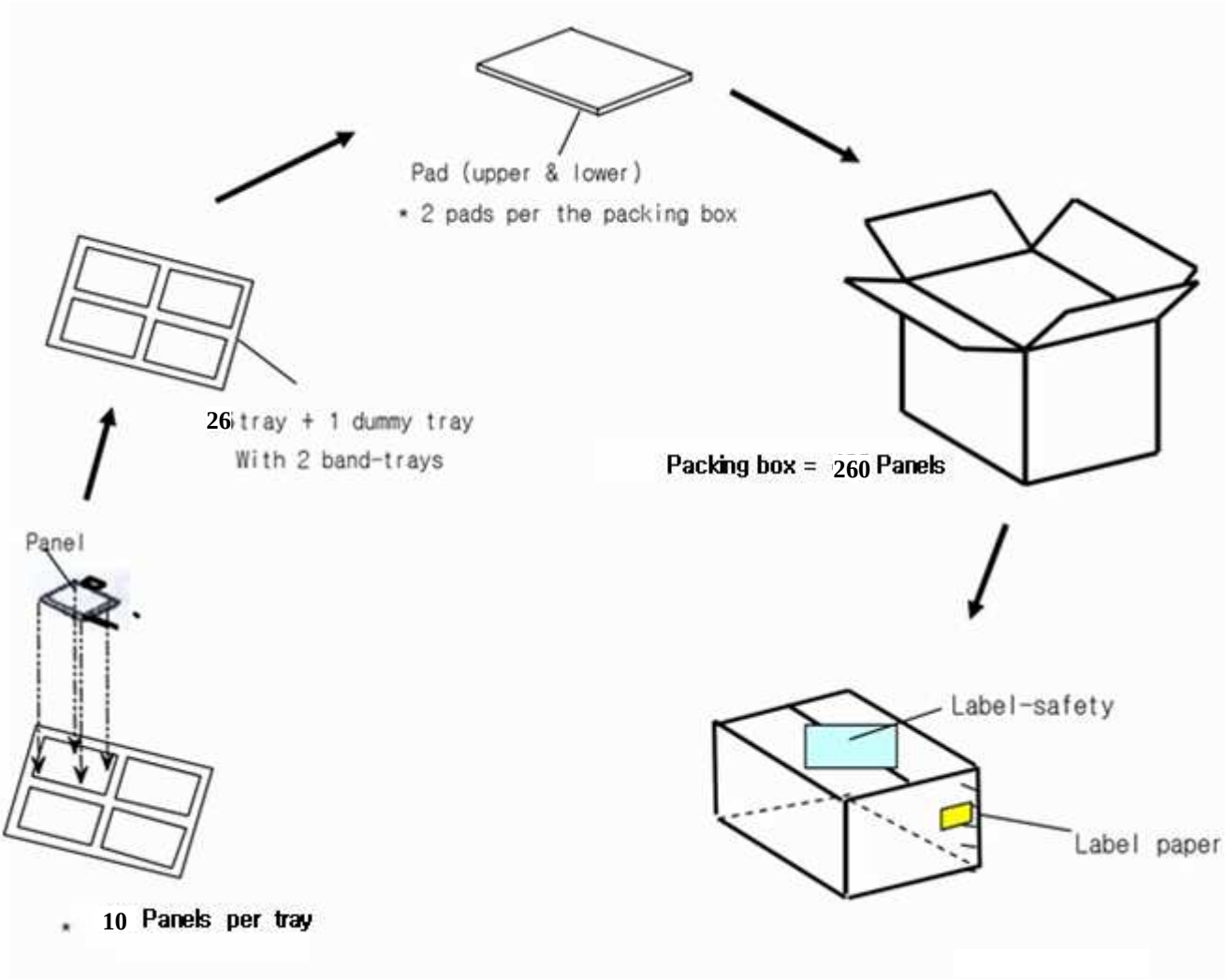
MODEL NAME	LMS350DF01(Blue Ocean)		
PART/SHEET NAME	Outline Dimension	SHEET	1/1
CODE NO.			

Samsung Confidential

심주환020205881225177167 20080909144125

306931220938848

12. Packing



Note (1) Packing Box Weight : Approx. 9.1 Kg

(2) Packing Box Size : 505(W) x 355(D) x 208(H)

(3) Place the panels in the tray facing the direction shown in the figure.

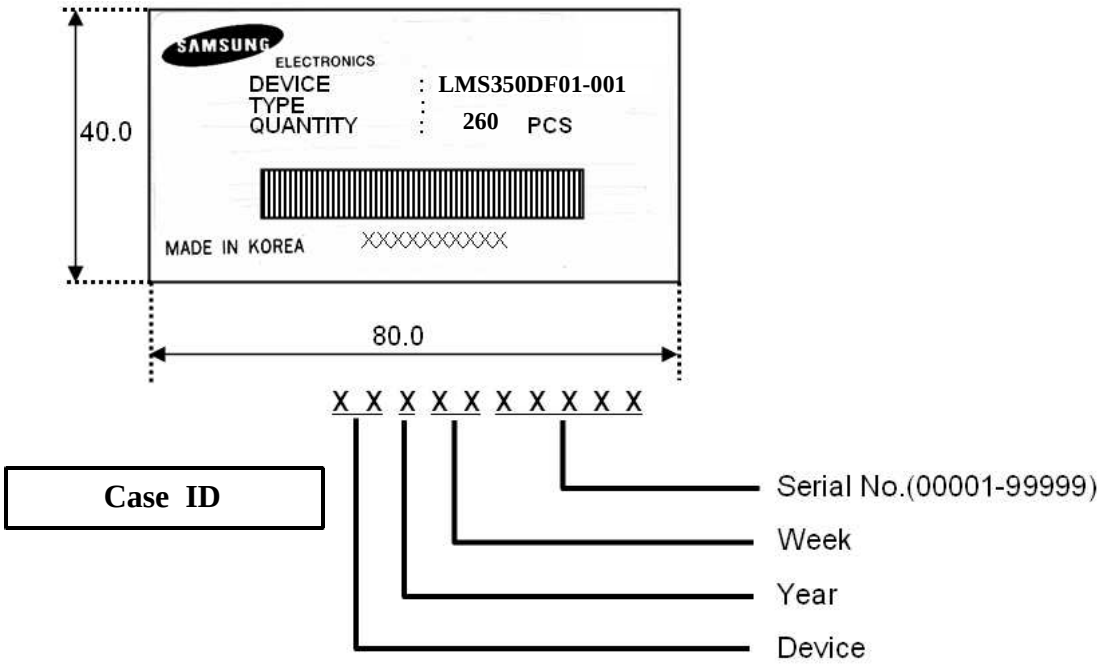
(4) Place 25 tray and 1 cover tray and 2 pads inside the packing-box

(5) Affix the label-safety, label-paper.

심주환020205881225177167 20080909144125
306931220938848

13. Marking & Others

(1) Packing case attach



심주환020205881225177167 20080909144125
306931220938848

14. General Precautions

14.1 Handling

(a) When the module is assembled, it should be attached to the system firmly. Be careful not to twist and bend the module.

(b) Refrain from strong mechanical shock and / or any force to the module. In addition to damage, this may cause improper operation or damage to the module and back-light unit.

(c) Note that polarizers are very fragile and could be easily damaged. Do not press or scratch the surface harder than a HB pencil lead.

(d) Wipe off water droplets or oil immediately. If you leave the droplets for a long time, Staining and discoloration may occur.

(e) If the surface of the polarizer is dirty, clean it using some absorbent cotton or soft cloth.

(f) The desirable cleaners are water, IPA(Isopropyl Alcohol) or Hexane. Do not use Ketone type materials(ex. Acetone), Ethyl alcohol, Toluene, Ethyl acid or Methyl chloride. It might permanent damage to the polarizer due to chemical reaction.

(g) If the liquid crystal material leaks from the panel, it should be kept away from the eyes or mouth. In case of contact with hands, legs or clothes, it must be washed away thoroughly with soap.

(h) Protect the module from static, it may cause damage to the Integrated Gate Circuit.

(i) Use finger-stalls with soft gloves in order to keep display clean during the incoming inspection and assembly process.

(j) Do not disassemble the module.

(k) Protection film for polarizer on the module shall be slowly peeled off just before use so that the electrostatic charge can be minimized.

(l) Pins of I/F connector shall not be touched directly with bare hands

심주환020205881225177167 20080909144125
306931220938848

14.2 Storage

(a) Do not leave the panel in high temperature, and high humidity for a long time. It is highly recommended to store the module with temperature from 0 to 35°C and relative humidity of less than 70%.

(b) Do not store the TFT-LCD module in direct sunlight.

(c) The module shall be stored in a dark place. It is prohibited to apply sunlight or fluorescent light during the store.

14.3 Operation

(a) Do not connect, disconnect the module in the "Power On" condition.

(b) Power supply should always be turned on/off by the "Power on/off sequence"

14.4 Others

(a) The Liquid crystal is deteriorated by ultraviolet, do not leave it in direct sunlight and strong ultraviolet ray for many hours.

(b) Avoid condensation of water. It may result in improper operation or disconnection of electrode.

(c) Do not exceed the absolute maximum rating value. (the supply voltage variation, input voltage variation, variation in part contents and environmental temperature, and so on) Otherwise the panel may be damaged.

(d) If the panel displays the same pattern continuously for a long period of time, it can be the situation when the image "Sticks" to the screen.

(e) This panel has its circuitry FPC on the bottom side and should be handled carefully in order not to be stressed.

심주환020205881225177167 20080909144125
306931220938848